Claims

1. A data transfer method for a digital image processing apparatus, comprising the steps of:

converting first binary voltage data of n-bit (n is an integer equal to or larger than two) to multi-value current data of 2^n values;

transferring the multi-value current data through a single data line;

converting the multi-value current data on the data line to binary current data of (2^n-1) bits;

converting the binary current data of the (2^n-1) bits to second binary voltage data of (2^n-1) bits; and

restoring the first binary voltage data of the n bits from the second binary voltage data of the (2^n-1) bits.

2. A data transfer circuit for a digital image processing apparatus, comprising:

a voltage/current converter circuit for converting first binary voltage data of n-bit (n is an integer equal to or larger than two) to multi-value current data of 2^n values;

a single data transfer line for transferring the multi-value current;

a current comparator circuit for converting the multi-value current data on the data line to binary current data of (2^n-1) bits;

a current/voltage converter circuit for converting the binary current data of the (2^n-1) bits to second binary voltage data of (2^n-1) bits; and

a counter circuit for restoring the first binary voltage data of the n bits from the second binary voltage data of the (2^n-1) bits.

3. A data transfer circuit according to claim 2, wherein:

said voltage/current converter circuit generates a current proportional to a value 2^i (i is an integer equal to or larger than zero and equal to or smaller than n-1) corresponding to each bit of the n bits, and multiplexes the generated currents to output the multi-value current data of the 2n bits having a current value proportional to the first binary voltage data of the n bits on the data transfer line.

4. A data transfer circuit according to claim 2 or 3, wherein:

said current comparator circuit expands the multi-value current data to (2n-1) bits, and outputs the binary current data of the (2^n-1) bits, the logical values of which are determined based on whether or not a current value of the multi-value current data is larger than a corresponding threshold current at each of the (2^n-1) bits.

5. A data transfer circuit according to any of claims 2 to 4, wherein:

said current/voltage converter circuit converts the binary current data of the (2^n-1) bits to the second binary voltage data of the (2^n-1) bits in units of bits.

6. A data transfer circuit according to any of claims 2 to 5, wherein:

said counter circuit comprises a logic circuit which receives the second binary voltage data of the (2^n-1) bits, and restores the first binary voltage data based on positions of bits which have logical "1."

7. A data transfer circuit according to claim 3, wherein:

said voltage/current converter circuit comprises a group of first circuits arranged in parallel in correspondence to the n bits, and

each of said first circuits generates a current proportional to a value 2^i (i is an integer equal to or larger than zero and equal to or smaller than n-1) corresponding to a corresponding bit of the n bits.

8. A data transfer circuit according to claim 7, wherein:

each of said first circuits comprises:

a first transistor having a source terminal connected to a power supply terminal or a ground terminal, and a gate terminal and a drain terminal connected to each other;

a second transistor applied at a gate with first binary voltage data of the corresponding bit of the n bits from the outside, and having a drain terminal connected to the drain terminal of the first transistor; and

a third transistor having a source terminal connected to the power supply terminal or the ground terminal, and a gate terminal connected to the gate terminal of said first transistor,

said voltage/current converter circuit further comprises a first constant current source connected between the source terminal of said second transistor in each of said first circuits and the ground terminal or the power supply terminal, and

said third transistor in each of said first circuits has a drain terminal connected to the data transfer line in common.

9. A data transfer circuit according to claim 8, wherein:

said third transistor in each of said first circuits has the gate terminal, the size of which is set to have an output current value proportional to 2^i in accordance with the first binary voltage data of n bits supplied from the outside.

10. A data transfer circuit according to claim 4, wherein:

said current comparator circuit comprises a group of second circuits arranged in parallel in correspondence to the (2^n-1) bits, and

each of said second circuits sets a logical value of a corresponding bit to "1" when a current value of the multi-value current data is larger than a corresponding threshold current.

11. A data transfer circuit according to claim 10, wherein:

said current comparator circuit comprises a fourth transistor which receives the multi-value current data at a drain, and has a gate terminal connected to the drain terminal, and a source terminal connected to a ground terminal or a power supply terminal, and said group of second circuits, and

each of said second circuits comprises:

a fifth transistor having a gate terminal connected to the gate terminal of said fourth transistor, a source terminal connected to a common ground terminal or a common power supply terminal; and

a second constant current source connected between

the drain terminal of said fifth transistor and the power supply terminal or the ground terminal for applying the threshold current, and

said current comparator circuit outputs the second binary current data of the (2^n-1) bits, the logical value of which is set to "1" from LSB to a bit corresponding to the threshold current.

12. A data transfer circuit according to claim 11, wherein:

said second constant current source applies different threshold currents of the (2^n-1) bits in predetermined step units, and

said current comparator circuit outputs binary current data of (2^n-1) bits which has a bit corresponding to the largest threshold current at MBS, and a bit corresponding to the smallest threshold current at LSB.

13. A data transfer circuit according to claim 5, wherein:

said current/voltage converter circuit comprises a group of third circuits arranged in parallel in correspondence to the (2^n-1) bits of the binary current data, respectively, and

each of the third circuits converts a corresponding bit of the binary current data of the (2^n-1) bits to a corresponding bit of the second binary voltage data of (2^n-1) bits.

14. A data transfer circuit according to claim 13, wherein:

said current/voltage converter circuit comprises a third constant current source and said group of third

circuits, and

each of said third circuits comprises:

a sixth transistor having a source terminal connected to a common power supply terminal or a common ground terminal, and a gate terminal connected to a drain terminal; and

a seventh transistor having a gate terminal for receiving the binary current data of a corresponding bit of the (2^n-1) bits, a source terminal connected to said third constant current source, and a drain terminal connected to the drain terminal of said sixth transistor.

15. A data transfer circuit according to claim 6, wherein:

said counter circuit comprises a logic circuit for restoring the first binary voltage data of the n bits which have all bits at logical "0" when all the bits of the second binary voltage data of the (2^n-1) bits are logical "0," and restoring the first binary voltage data of the n bits corresponding to a binary number of the number of bits of logical "1" from LSB of the second binary voltage data of the (2^n-1) bits.

16. A data transfer circuit according to claim 15, wherein:

said counter circuit comprises a bit determination circuit for three least significant bits, and

said bit determination circuit comprises:

a first 3-bit input AND circuit for outputting logical "1" when the three least significant bits are logical "1";

a second 3-bit input AND circuit for outputting logical "1" when only a third bit is logical "1"; and

an OR circuit for calculating a logical OR of the output of said first 3-bit input AND circuit and the output of said second 3-bit input AND circuit.

17. An output circuit comprising:

an input unit for receiving binary voltage data X_i (i is an integer equal to or larger than zero and equal to or smaller than n-1) of n bits (n is an integer equal to or larger than two); and

a group of current mirror circuits for outputting current values proportional to 2^i,

wherein the output currents of said group of current mirror circuits are multiplexed to generate a current value proportional to $\Sigma 2^i X_i$ in accordance with the binary voltage data X_i.

18. An output circuit comprising:

an input unit for receiving binary voltage data X_i (i is an integer equal to or larger than zero and equal to or smaller than n-1) of n bits (n is an integer equal to or larger than two);

a first transistor provided for each bit of the n bits of the binary voltage data X_i, and having a source terminal connected to a power supply terminal or a ground terminal, and a gate terminal and a drain terminal connected to each other;

a second transistor provided for said each bit, applied with the binary voltage data X_I at a gate terminal, and having a drain terminal connected to the drain terminal of said first transistor;

a third transistor provided for said each bit, and having a source terminal connected to the power supply terminal or the ground terminal, a gate terminal connected

to the gate terminal of said first transistor, and a drain terminal connected to a multi-value current data output line; and

a constant current source provided for said each bit, and connected between the source terminal of said second transistor and the ground terminal or the power supply terminal,

wherein said output circuit outputs multi-value current data having a current value proportional to $\Sigma 2^i X_i$ to said multi-value current data output line in accordance with the binary voltage data X_i.

19. An output circuit comprising:

sets of first transistors to third transistors arranged in parallel, corresponding respectively to n bits (n is an integer equal to or larger than two) of binary voltage data Xi (i is an integer equal to or larger than zero and equal to or smaller than n-1) of the n bits supplied from the outside,

wherein said first transistor and said third transistor have source terminals connected to a common power supply terminal or a common ground terminal, said second transistor has a source terminal connected to a common regulated current, said third transistor has a drain connected to a common multi-value current data line, and a current value proportional to $\Sigma 2^i X_i$ in accordance with the binary voltage data X_i is output to the common multi-value current data output line.

20. An output circuit according to claim 19, wherein:

said third transistor has a size which is set to generate an output current value proportional to 2^i in accordance with the binary voltage data X_i.

21. An input circuit comprising:

a current comparator circuit; and

a current/voltage converter circuit,

wherein said current comparator circuit comprises:

an input unit for receiving single multi-value current data of 2^n values (n is an integer equal to or larger than 2);

(2^n-1) independent current mirror circuits, said multi-value current data being expanded to said (2^n-1) current mirror circuits; and

(2^n-1) threshold current sources for supplying threshold currents corresponding to the 2^n value of the multi-value current data to said (2^n-1) current mirror circuits, respectively, and

binary voltage data of a corresponding bit of (2^n-1) bits is output based on current driving capabilities of each of said (2^n-1) current mirror circuits and the threshold current from a corresponding one of said (2^n-1) threshold current sources, and

said current/voltage converter circuit converts the binary current data of the (2^n-1) bits to binary voltage data of the (2^n-1) bits.

22. An input circuit according to claim 21, wherein:

said current comparator circuit comprises:

a fourth transistor provided for each bit of the (2^n-1) bits, applied with the multi-value current data at a drain terminal, and having a gate terminal connected to the drain terminal, and a source terminal connected to a common ground terminal or a common power supply terminal;

a fifth transistor provided for said each bit, and having a gate terminal connected to the gate terminal of

said fourth transistor, and a source terminal connected to the common ground terminal or the common power supply terminal; and

a constant current source provided for said each bit and connected between the drain terminal of said fifth transistor and the common power supply terminal or the common ground terminal.

23. An input circuit comprising:

a current comparator circuit; and

a current/voltage converter circuit,

wherein said current comparator circuit comprises:

(2^n-1) sets of a fifth transistor arranged in parallel to a single multi-value current data input of 2^n values (n is an integer equal to or larger than two) supplied from the outside, and a threshold current source for outputting a threshold current used to discriminate the multi-value current data,

said current comparator circuit has said fifth transistor having a source terminal connected to a common ground terminal or a common power supply terminal, and said threshold current source connected to a common power supply terminal or a common ground terminal, and outputs binary current data of (2^n-1) bits based on the multi-value current data and the threshold current from said threshold current source, and

said current/voltage converter circuit converts the binary current data of the (2^n-1) bits to binary voltage data of the (2^n-1) bits.

24. An input circuit according to claim 23, wherein:

said current comparator circuit detects a bit corresponding to the multi-value current data within the

(2^n-1) bits based on a drain current of said fifth transistor and the threshold current of said threshold current source, and outputs the binary current data of the (2^n-1) bits having a bit corresponding to the largest threshold current at the most significant bit.

25. An input circuit according to any of claims 21 to 24, wherein:

said current/voltage converter circuit comprises:

(2^n-1) circuit units arranged in parallel to the binary current data inputs of the (2^n-1) bits,

each of said (2^n-1) circuit units comprises a sixth transistor and a seventh transistor,

said sixth transistor has a source terminal connected to the common power supply terminal or the common ground terminal, and said sixth transistor has a gate terminal and a drain terminal connected to each other,

said seventh transistor has a source terminal connected to a third constant current source, said seventh transistor is applied with the binary current data of a corresponding bit of the (2^n-1) bits at a gate terminal, and the binary voltage data of the corresponding bit is output from the drain terminal of said sixth transistor connected to the drain terminal of said seventh transistor.

26. An input circuit according to claim 25, wherein:

said third constant current source is set to output the binary voltage data having a voltage level indicative of logical "0" or "1" for each of the (2^n-1) bits of the binary current data, and

said current/voltage converter circuit outputs the binary voltage data of the (2^n-1) bits having binary voltage data corresponding to binary current data at the

most significant bit at the most significant bit, and binary voltage data corresponding to binary current data at the least significant bit at the least significant bit.

27. A semiconductor device comprising the output circuit according to any of claims 17 to 20.

28. A semiconductor device comprising the input circuit according to any of claims 21 to 26.

29. An electronic apparatus comprising the output circuit according to any of claims 17 to 20, wherein the single multi-value current data is output from said output circuit.

30. An electronic apparatus comprising the input circuit according to any of claims 21 to 26, for converting the single multi-value current data supplied from the outside to binary voltage data.